REMARKS

Claims 32-53 and 58-61 are pending, with claims 32, 36, 38, 42, 44, 45, 47, 48, 58, and 61 being in independent form.

At the outset, Applicant acknowledges with appreciation the indication of allowable subject matter, and the withdrawal of the prior-raised claim rejections.

In the Office Action, claims 32-35 and 58-60 stand newly rejected for anticipation by European Patent Application Publication No. EP 0 741 391 A2 to Itakura et al. ("Itakura"). Applicant believes the rejected claims are novel and inventive in view of the cited document for the following reasons.

Anticipation requires that every feature of the claimed invention be shown in a single prior document. In re Paulsen, 30 F.3d 1475 (Fed. Cir. 1994); In re Robertson, 169 F.3d 743 (Fed. Cir. 1999). The pending claims positively recite features that are not described in the cited document.

For example, claim 32, recites, among other things, "an integrator for integrating *the analog input signal* during a sampling phase" (emphasis added). Similarly, method claim 58 recites "integrating an analog input signal during a sampling phase". Accordingly, claims 32 and 58 define that the integrator operates directly on the analog input signal during the sampling phase. This interpretation is supported throughout the specification, and particularly in FIG. 1A, where Applicant shows the input of the integrator 3 being directly connected to the analog input signal (INPUT) via the sampling switch 2.

In contrast, the arrangement described in Itakura includes a sample-and-hold (S/H) circuit, illustrated in FIG. 1, having an integrator that is *not* directly connected to the analog input signal. At col. 6, l. 25 et seq., Itakura describes that the S/H circuit includes an input terminal 54 connected to a capacitor 57 *through a Schottky diode 56*. This arrangement is clearly shown in the figure as well. The Action asserts that the capacitor 57 integrates the analog input signal presented at the input terminal 54 during the sampling phase, but as is shown in the figure, the capacitor 57 integrates a signal that is conditioned by the Schottky diode 56. Accordingly, claim 32 does not read on Itakura's S/H circuit as the Action asserts, and is believed to be allowable for at least this reason.

The feature of "integrating the analog input signal during a sampling phase", which is absent from Itakura's arrangement, is not insignificant. As shown in FIG. 3 of Itakura and described in the corresponding text, the Schottky diode 56 results in the S/H

circuit shown in FIG. 1 operating more like a traditional voltage sampler, such as that described in the background section of this application. Itakura describes that when the MOS transistor 55 is shut off, the Schottky diode 56 becomes reverse biased, and can be represented by the equivalent circuitry shown in FIG. 3. The Schottky capacitance 62 helps to isolate error signals from propagating from the transistor 55 to the output 59. As described at col. 2, l. 46 et seq., these error signals can cause the picture quality in liquid crystal displays (LCDs), incorporating a large number of such S/H circuits, to deteriorate. As discussed in the background section of this application, voltage sampling S/H arrangements similar to that described by Itakura can limit the bandwidth of analog-to-digital (A/D) converters that use such S/H circuitry.

Claim 33 recites, among other things, "a sampling switch having a signal input for analog input signals, *a signal output connected to a signal input of said integrator*" (emphasis added). For reasons similar to those discussed above, claim 33 does not read on the arrangement described in Itakura. In particular, Itakura does not describe an arrangement in which the signal output of the sampling switch is connected to a signal input of the integrator. Instead, Itakura describes an arrangement in which the signal output of the sampling switch transistor 55 is connected to a Schottky diode 56. Accordingly, claim 33 is believed to be allowable over the cited document for this reason as well.

With respect to claim 35, the Action asserts that all of the claimed features are inherently described by Itakura's S/H circuit arrangement. Applicant respectfully disagrees. Claim 35 recites, among other things, the feature "wherein if said sampling phase is from time t_1 to t_2, said sample represents the instant value of said analog signal at time $t_s = (t_1 + t_2) / 2$". Applicant describes on p. 7, l. 35, through p.8, l. 5, of the specification that:

> During the sampling phase, only the sampling switch 2 is turned on, and the signal current is integrated onto the capacitor 3-1. The time constant [of the integrator] is large enough to be able to obtain *a linear charging* when the signal comes from a voltage source (the usual case). If the on-resistance of the switch 2 is too small, the optional resistor 303 can be added [to the integrator]. (emphasis added).

Choosing a time constant that is large enough to be able to obtain a linear charging of the capacitor 3-1 can allow an i^{th} frequency component of the input signal to be sampled precisely at time $t_s = (t_1 + t_2) / 2$, or at the midpoint of the sampling window. Consequently, since all frequency components of the input signal are sampled at time t_s,

the total charge on the capacitor 3-1 naturally represents the signal sampled at the sampling time t_s (see pg. 8, ll. 26-31, of the specification).

In contrast, FIG. 4 of Itakura shows that the sampled value 633 does *not* represent the instant value of the analog signal 631 at the midpoint of the sampling phase "d", as claim 35 requires. This, in turn, is true because Itakura's arrangement does not provide for a linear charging of the capacitor 57 during the sampling phase, as evidenced by the sampled value 633 and anode terminal 632 waveforms shown in FIG. 4. Accordingly, claim 35 is believed to be allowable for this reason as well.

In view of the above, claims 32, 33, and 35 are believed to be allowable over the cited document. Claim 58, which recites features similar to the absent features identified in arguing for the patentability of claim 32, is believed to be allowable as well. Moreover, the remaining rejected claims in application, which ultimately depend from one of claims 32 and 58, are believed to be allowable for at least these same reasons. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the anticipation rejection raised in the Action.

For the foregoing reasons, Applicant believes the application is in condition for allowance, and respectfully requests a Notice to this effect be provided at an early date. If any questions remain, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,

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